In the Claims:

1. (Original) A method of amplifying a signal by a transistor of an array of transistors including a storage cell transistor array of a dynamic random access memory (DRAM), comprising:

providing an array of transistors including transistors of a storage cell transistor array of a dynamic random access memory array;

connecting one of a source and a drain of a transistor of said array of transistors to a fixed potential; and

applying an input signal to a gate of said transistor,

whereby said transistor amplifies said input signal to provide an output signal appearing on the other of the source and the drain of said transistor.

2. (Original) The method of claim 1 wherein said fixed potential is ground, said input signal is applied as a voltage signal to said gate, and said output signal is inverted relative to said input signal.

3. (Original) The method of claim 1 wherein said fixed potential is a supply voltage, said input signal is applied to said gate as a voltage signal, and said output signal is non-inverted relative to said input signal.

4. (Original) The method of claim 1 wherein said input signal comprises a data bit signal from a bitline coupled to a storage cell currently accessed by said storage cell transistor array.

5. (Original) The method of claim 4 further comprising applying said output signal of said transistor as input to a sense amplifier external to said storage cell transistor array.

6. (Original) The method of claim 5 further comprising applying a reference signal as input to said sense amplifier, and differentially sensing a value of said output signal of said transistor in relation to said reference signal.

7. (Original) The method of claim 6 wherein said reference signal is generated by a reference transistor having a gate to which a reference voltage is applied.

8. (Original) The method of claim 7 wherein said reference voltage is a DC voltage.

9. (Original) The method of claim 7 wherein said reference voltage is applied to said gate of said reference transistor by a reference bitline of said storage cell array.

10. (Original) The method of claim 9 further comprising allowing a voltage of said reference bitline to float when applying said output signal of said transistor as input to said sense amplifier.

11. (Original) The method of claim 10 wherein said array of transistors include vertically oriented transistors and said transistor comprises a transistor of said vertically oriented transistors.

12. (Original) The method of claim 4 further comprising selecting said output signal from a plurality of signals output from a plurality of transistors including said transistor, and coupling said selected output signal to a sense amplifier external to said storage cell transistor array.

13. (Original) The method of claim 1 further comprising forming a well within a semiconductor substrate by a sequence of steps applied uniformly throughout a region of said semiconductor substrate, wherein said array of transistors including transistors of said storage cell transistor array are provided within said well.

14. (Original) An apparatus for amplifying a signal, comprising:

a first transistor of an array of transistors including transistors of a storage cell transistor array, all of said transistors of said array of transistors being located in a first well of a single crystal semiconductor substrate, said first transistor having a first source-drain region coupled to a fixed potential, a second source-drain region coupled to a conductive line, and a gate coupled to receive an input signal to be amplified,

whereby said first transistor is operable to amplify the input signal to provide an output signal onto said conductive line.

15. (Original) The apparatus of claim 14 wherein said fixed potential is ground, said input signal is a voltage signal and said output signal is inverted relative to said input signal.

16. (Original) The apparatus of claim 14 wherein said fixed potential is a supply voltage, said input signal is a voltage signal, and said output signal is not inverted relative to said input signal.

17. (Original) The apparatus of claim 14 wherein said input signal comprises a data bit signal from a bitline coupled to a source-drain region of a storage cell transistor of said storage cell transistor array.

18. (Original) The apparatus of claim 17 wherein said output signal is coupled to a sense amplifier external to said storage cell array.

19. (Original) The apparatus of claim 18 further comprising a second transistor of said array of transistors, said second transistor having a first source-drain region coupled to said bitline, a second source-drain region conductively coupled to said sense amplifier, and a gate coupled to a writeback control input,

whereby said second transistor is responsive to said writeback control input to apply a writeback signal from said sense amplifier to said bitline.

20. (Original) The apparatus of claim 14 wherein said array of transistors includes vertically oriented transistors and said first transistor comprises a transistor of said vertically oriented transistors.

21. (Currently amended) The apparatus of ~~claim 20~~ claim 19 wherein said array of transistors includes vertically oriented transistors and wherein said second transistor comprises a transistor of said vertically oriented transistors.

22. (Original) The apparatus of claim 18 further comprising a selection transistor coupled between said first transistor and said sense amplifier, said selection transistor responsive to selection input to selectively connect said output signal of said first transistor to said sense amplifier.

23. (Original) The apparatus of claim 18 further comprising a reference transistor coupled to said sense amplifier, having a gate to which a reference voltage is applied.

24. (Original) The apparatus of claim 23 wherein said gate of said reference transistor is coupled to a reference bitline of said storage cell transistor array to provide said reference voltage.